LH53V4000

CMOS 4M (512K × 8/256K × 16)
Mask-Programmable ROM

FEATURES

- 524,288 words × 8 bit organization
  (Byte mode)
  262,144 words × 16 bit organization
  (Word mode)
- Access times:
  200 ns (MAX.) at 3.0 V ≤ V_{CC} < 4.5 V
  100 ns (MAX) at 4.5 V ≤ V_{CC} ≤ 5.5 V
- Power consumption:
  Operating:
  108 mW (MAX.) at 3.0 V ≤ V_{CC} ≤ 3.6 V
  225 mW (MAX.) at 3.6 V < V_{CC} < 4.5 V
  412.5 mW (MAX.) at 4.5 V ≤ V_{CC} ≤ 5.5 V
  Standby: 550 µA(MAX.)
- Static operation
- Three-state outputs
- Wide range power supply: 3.0 V to 5.5 V
- Packages:
  40 pin, 600-mil DIP
  40 pin, 525-mil SOP
  48 pin 12 × 18 mm^2 TSOP (Type I)

DESCRIPTION

The LH53V4000 is a 4M-bit mask-programmable ROM organized as 524,288 × 8 bits (Byte mode) or 262,144 × 16 bits (Word mode) that can be selected by $\overline{BYTE}$ input pin. It is fabricated using silicon-gate CMOS process.

PIN CONNECTIONS

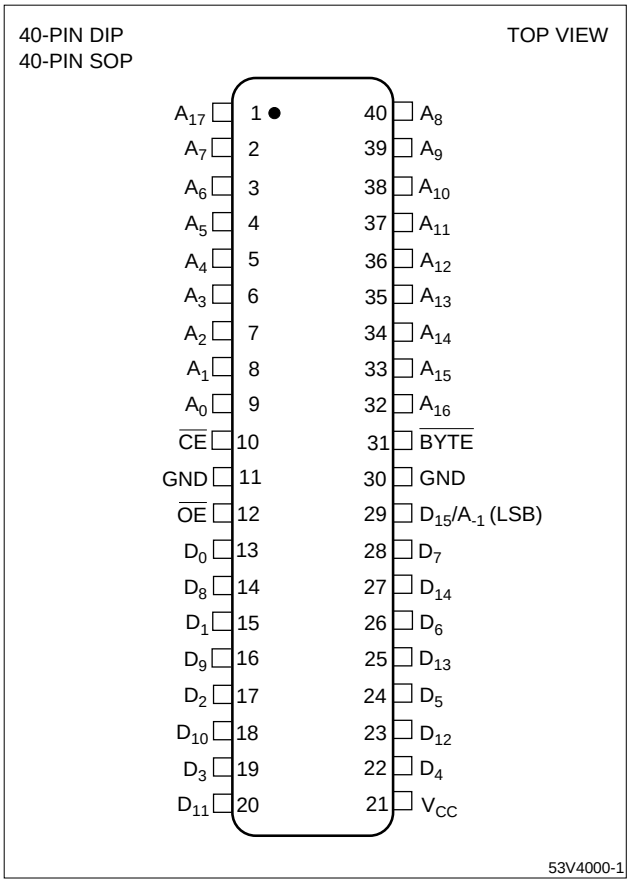


Figure 1. Pin Connections for DIP and SOP Packages

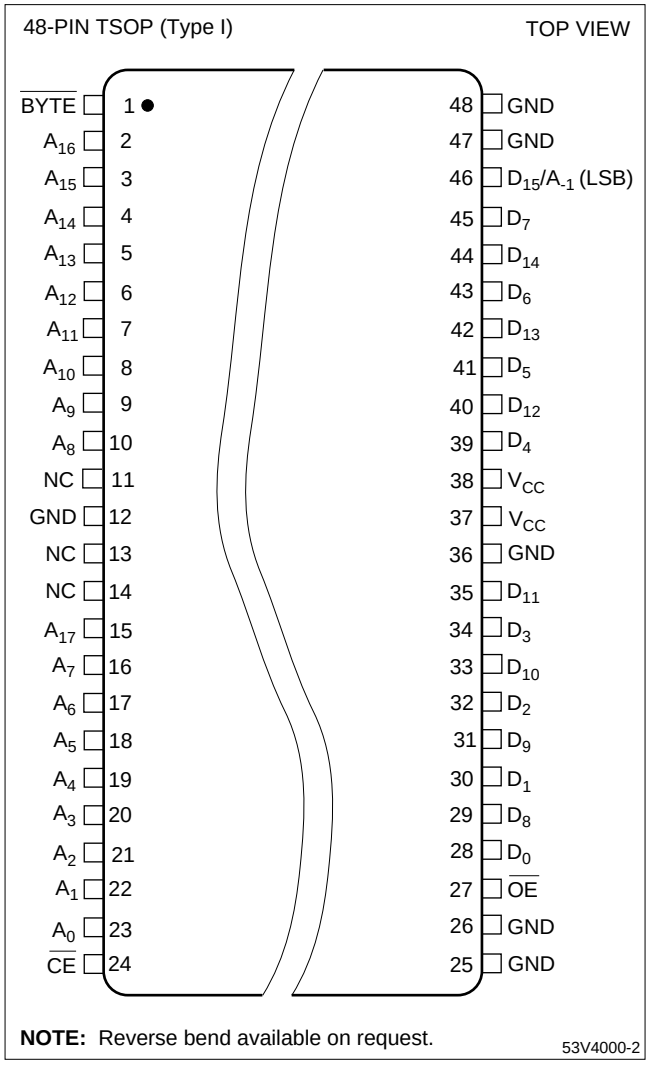


Figure 2. Pin Connections for TSOP Package

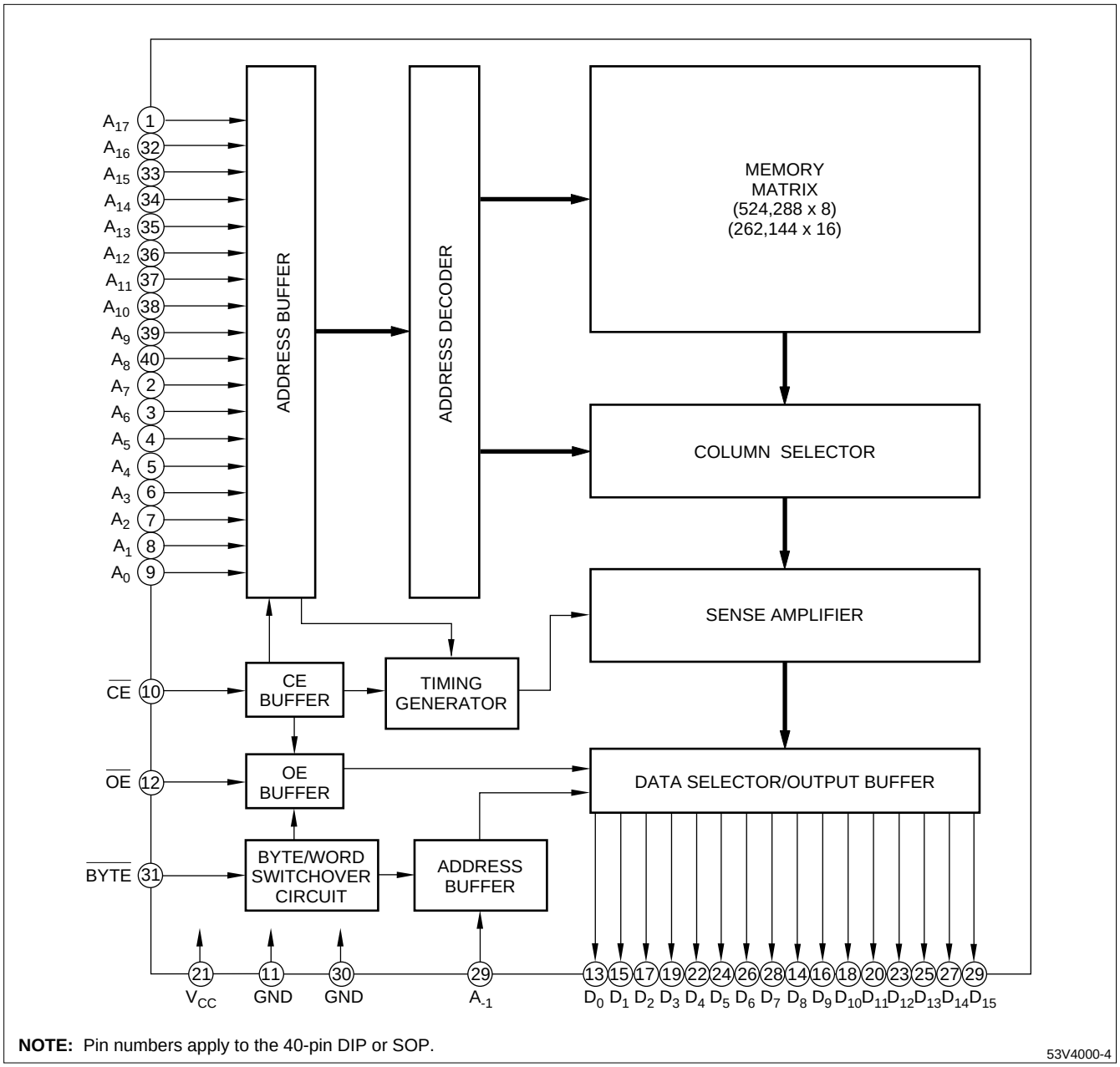


Figure 3. LH53V4000 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_{-1} - A_{17}	Address input	1
D_0 - D_{15}	Data output	1
$\overline{BYTE}$	Byte/word mode switch	1
$\overline{CE}$	Chip enable input	
$\overline{OE}$	Output enable input	
V_{CC}	Power supply (+5 V)	
GND	Ground	

NOTE:

1. The D_{15}/A_{-1} pin becomes LSB address input (A_{-1}) when the $\overline{BYTE}$ pin is set to be LOW in byte mode, and data output (D_{15}) when set to be HIGH in word mode.

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{BYTE}$	DATA OUTPUT		ADDRESS INPUT		SUPPLY CURRENT	NOTE
			D_0 - D_7	D_8 - D_{15}	LSB	MSB		
H	X	X	High-Z	High-Z	–	–	Standby	1
L	H	X	High-Z	High-Z	–	–	Operating	1
L	L	H	D_0 - D_7	D_8 - D_{15}	A_0	A_{17}	Operating	
L	L	L	D_0 - D_7	High-Z	A_1	A_{17}	Operating	

NOTES:
1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V_{CC}	–0.3 to +7.0	V
Input voltage	V_{IN}	–0.3 to V_{CC} + 0.3	V
Output voltage	V_{OUT}	–0.3 to V_{CC} + 0.3	V
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	3.0	–	5.5	V

DC CHARACTERISTICS (V_{CC} = 3.0 V to 5.5 V, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Input 'High' Voltage	V_{IH}		0.8 x V_{CC}	V_{CC} + 0.3	V	
Input 'Low' Voltage	V_{IL}		–0.3	0.4	V	
Output 'High' Voltage	V_{OH}	I_{OH} = –100 µA	0.8 × V_{CC}		V	
Output 'Low' Voltage	V_{OL}	I_{OL} = 400 µA		0.4	V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V, V_{CC}		10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V, V_{CC}		10	µA	1
Operating current	I_{CC1}	t_{RC} = 100 ns		75	mA	2
	I_{CC2}	t_{RC} = 200 ns		50	mA	3
	I_{CC3}	t_{RC} = 200 ns		30	mA	4
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}		3	mA	
	I_{SB2}	$\overline{CE}$ = V_{CC} – 0.2 V		100	µA	
Input Capacitance	C_{IN}	f = 1 MHz T_A = 25°C		10	pF	
Ouput Capacitance	C_{OUT}			10	pF	

NOTES:
1. $\overline{CE}/\overline{OE}$ = V_{IH}
2. 4.5 V ≤ V_{CC} ≤ 5.5 V, outputs open
3. 3.6 V < V_{CC} < 4.5 V, outputs open
4. 3.0 V ≤ V_{CC} ≤ 3.6 V, outputs open

AC ELECTRICAL CHARACTERISTICS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	3.0 V ≤ V_{CC} < 4.5 V		4.5 V ≤ V_{CC} ≤ 5.5 V		UNIT	NOTES
		MIN	MAX	MIN	MAX		
Read cycle time	t_{RC}	200		100		ns	
Address access time	t_{AA}		200		100	ns	
Chip Enable access time	t_{ACE}		200		100	ns	
Output Enable delay time	t_{OE}		120		55	ns	
Output hold time	t_{OH}	10		5		ns	
CE to output in High-Z	t_{CHZ}		100		40	ns	1
OE to output in High-Z	t_{OHZ}						

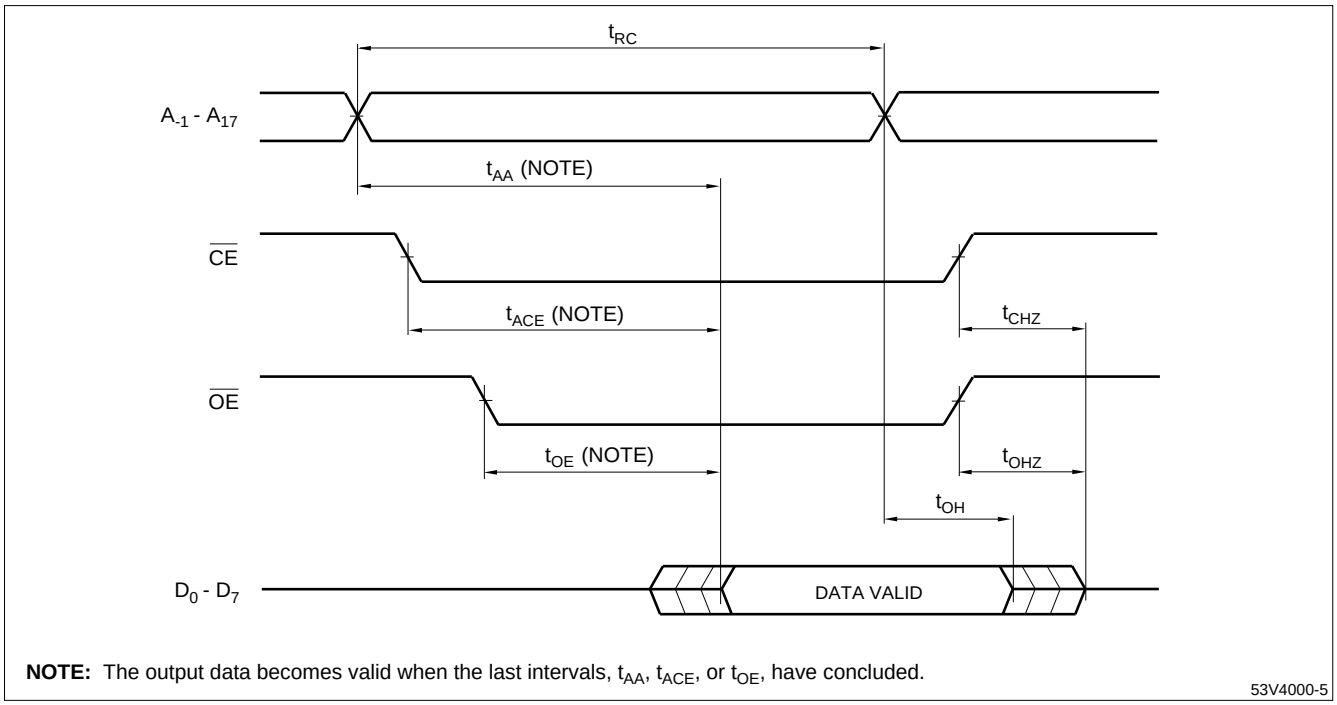
NOTE:
1. This is the time required for the outputs to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.4 V to (0.8 x V_{CC}) V
Input rise/fall time	10 ns
Input/output reference level	1.5 V
Output load condition	1TTL + 100 pF

CAUTION

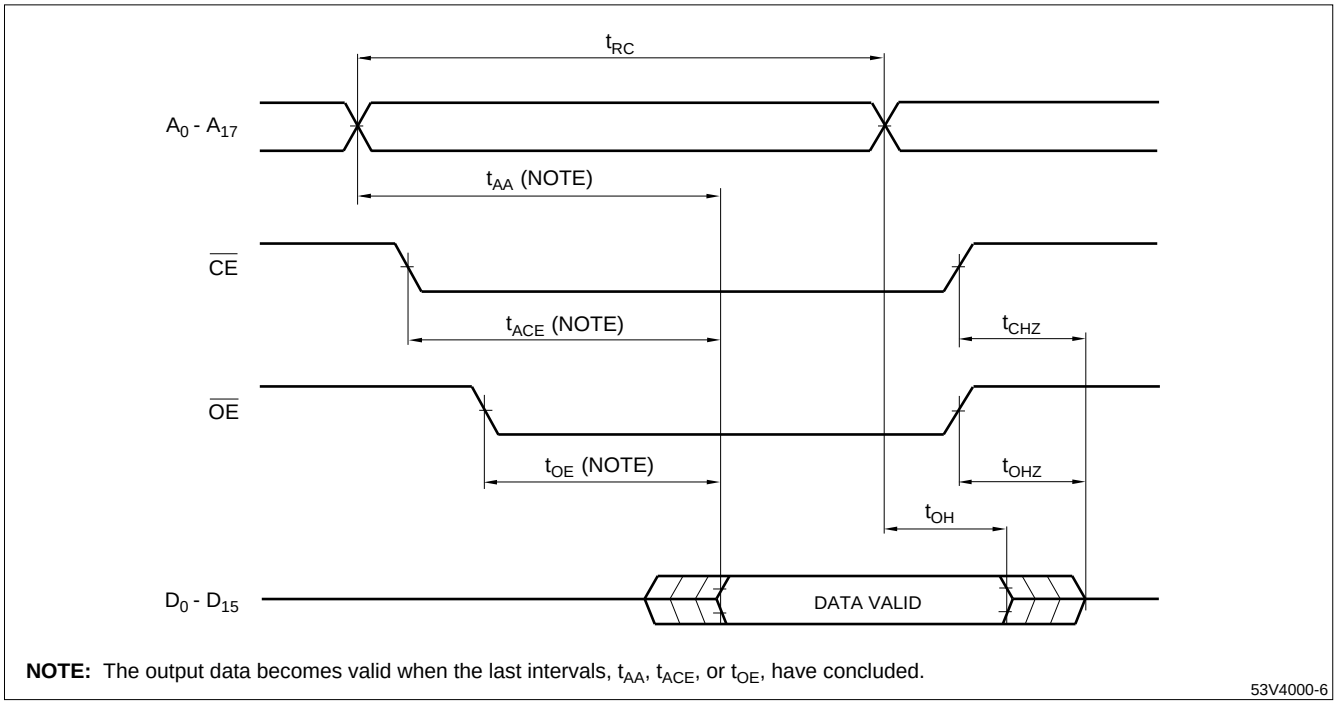
To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and the GND pin.



NOTE: The output data becomes valid when the last intervals, t_{AA}, t_{ACE}, or t_{OE}, have concluded.

53V4000-5

Figure 4. Byte Mode ($\overline{BYTE}$ = V_{IL})

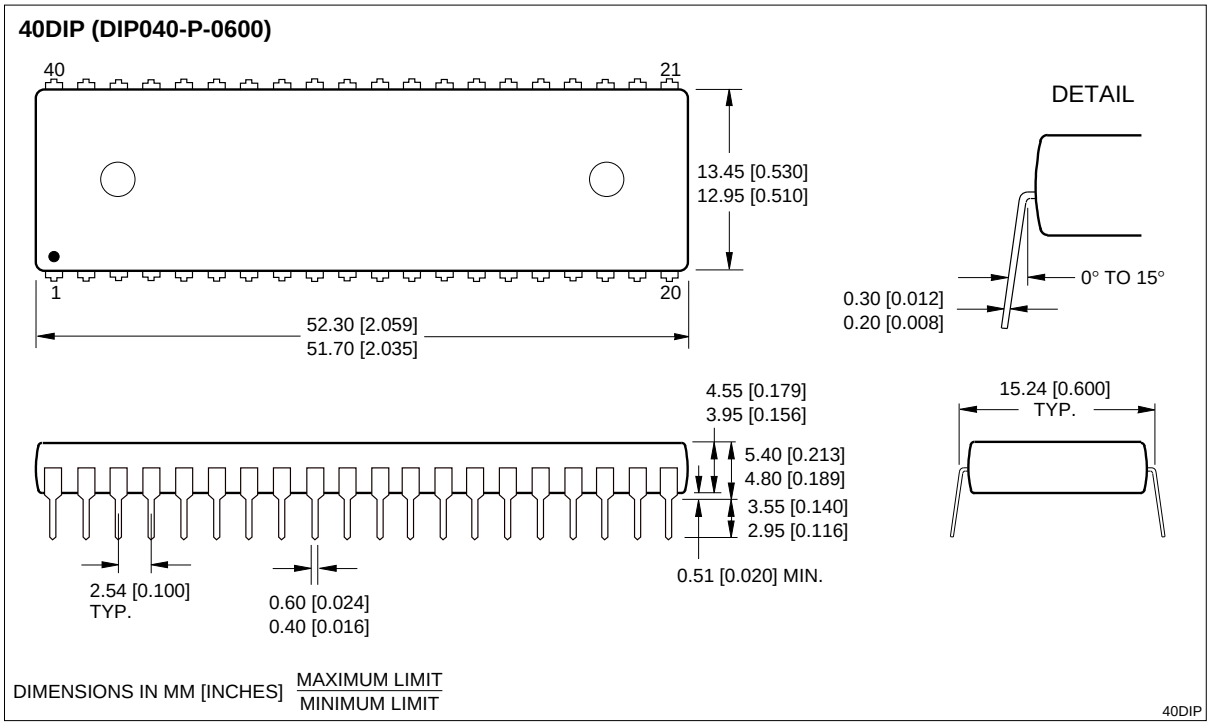


NOTE: The output data becomes valid when the last intervals, t_{AA}, t_{ACE}, or t_{OE}, have concluded.

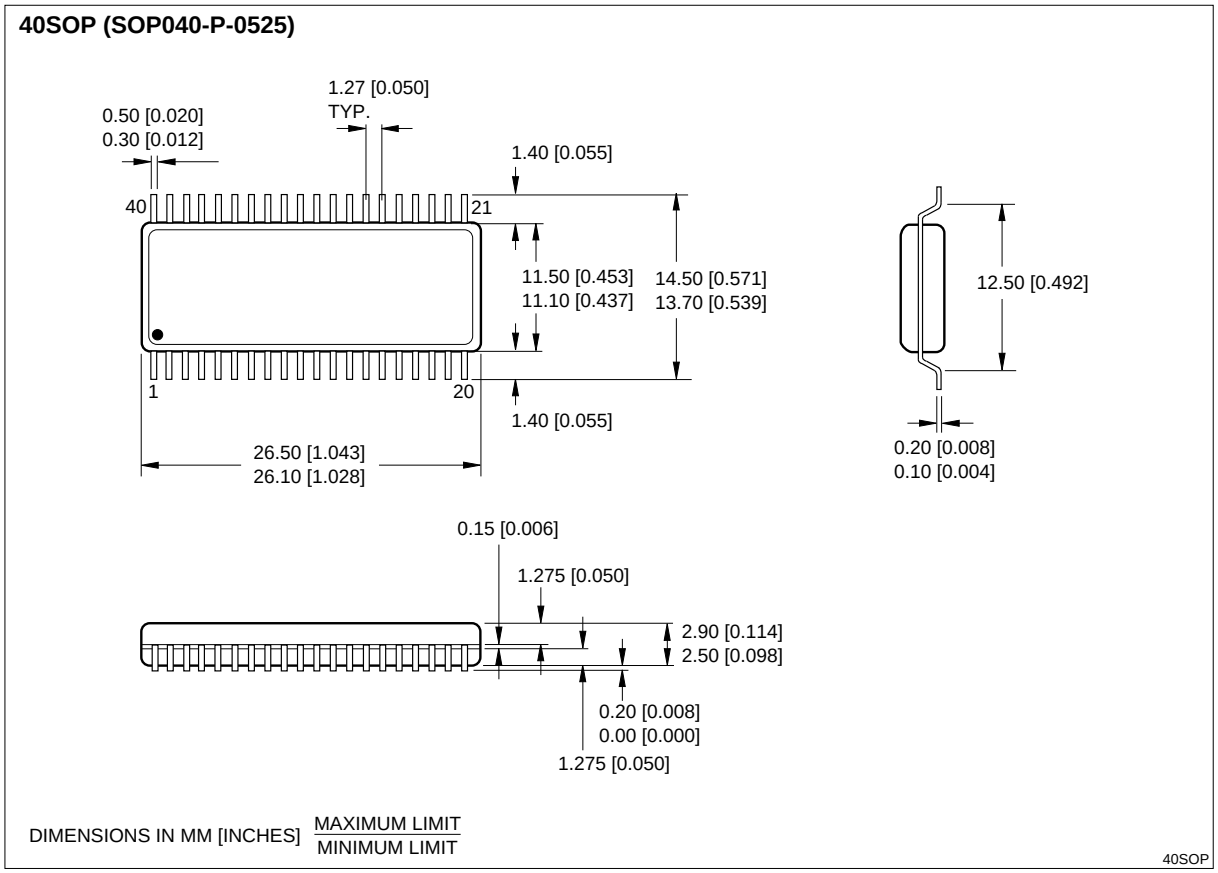
53V4000-6

Figure 5. Word Mode ($\overline{BYTE}$ = V_{IH})

PACKAGE DIAGRAMS

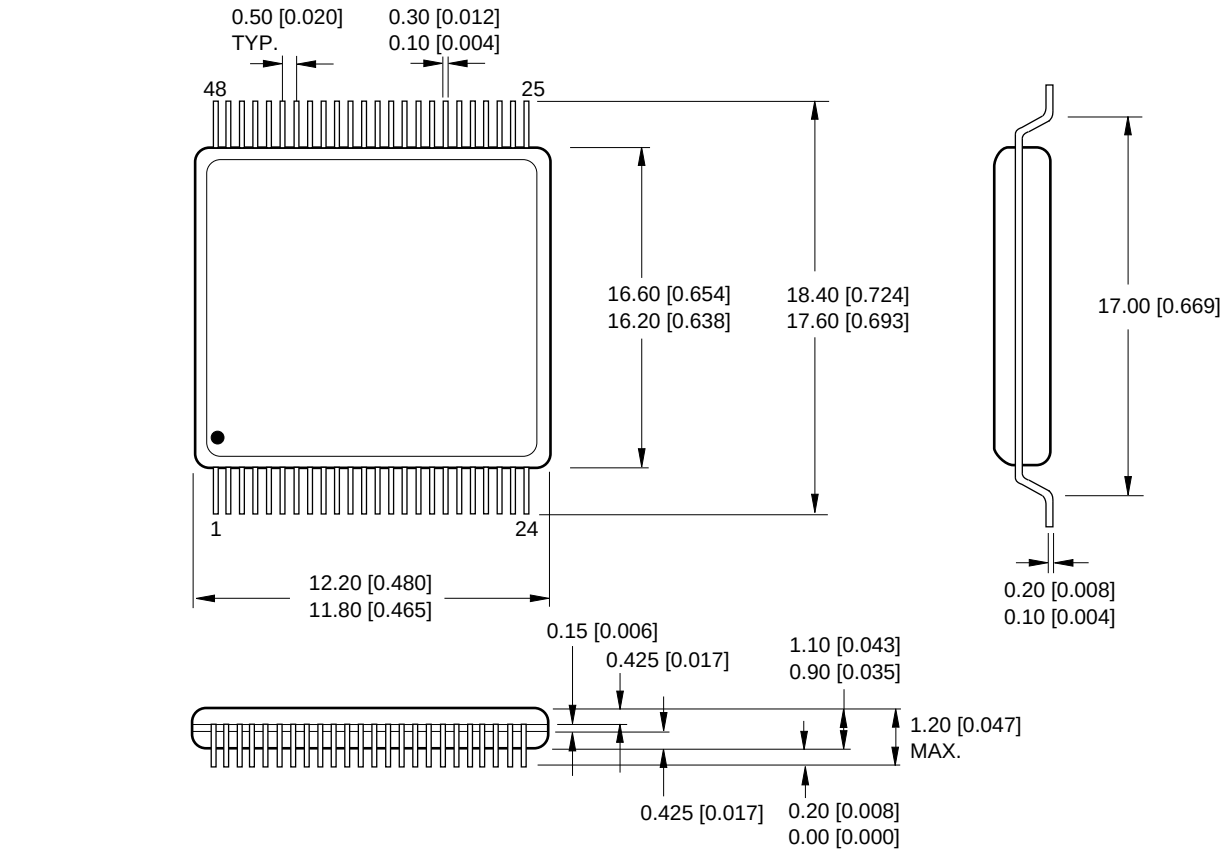


40-pin, 600-mil DIP



40-pin, 525-mil SOP

48TSOP (TSOP048-P-1218)



48-pin, 12 × 18 mm^2 TSOP (Type I)

ORDERING INFORMATION

LH53V4000 (Device Type) X (Package)

- D 40-pin, 600-mil DIP (DIP040-P-0600)
- N 40-pin, 525-mil SOP (SOP040-P-0525)
- T 48-pin, 12 x 18 mm^2 TSOP (Type I) (TSOP048-P-1218)
- TR 48-pin, 12 x 18 mm^2 TSOP (Type I) Reverse bend (TSOP048-P-1218)

LH53V4000 (Device Type): CMOS 4M (512K x 8 or 256K x 16) Mask-Programmable ROM

Example: LH53V4000D (CMOS 4M (512K x 8 or 256K x 16) Mask-Programmable ROM, 40-pin, 600-mil DIP)

53V4000-7